Feed-forward Compensation for Multilevel Cascaded H-bridge StatComs

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<<Multilevel Converters>>, <<Pulse Width Modulation>>, <<Static Synchronous Compensators>>

Abstract

Multilevel Static Compensators (StatComs) offer significant advantages over traditional two level converter based StatComs. The cascaded H-bridge topology for multilevel StatComs is increasing becoming the topology of choice. This paper will address the problem of compensating for the non-ideal nature of the H-bridges so that accurate current control can be achieved with this topology using a predictive current controller.

Introduction

Multilevel topologies, when applied to StatCom applications, have a three distinct advantages over the use of traditional two level converter topologies, namely:

- The presence of the multiple levels means that the filtering required on the StatCom output is significantly reduced. In fact, for high level numbers the filter only needs to be the grid connection inductor;
- For medium voltage levels multilevel StatComs can be directly connected to the grid without an expensive, lossy, and bulky interposing connection transformer;
- For high power levels, the fact that multilevel StatComs can operate at higher voltages means that the current rating of the power devices can be kept relatively low, and the lower harmonic content means that losses in the connection transformers can be reduced.

There are a number of topologies for multilevel StatComs – the flying capacitor topology, the neutral point clamped topology, the cascaded H-bridge topology, and a variety of hybrid topologies [1]. The University of Newcastle-Australia, and its joint venture company ResTech Pty Ltd are current developing a 19 level StatCom based on cascaded H-bridge converters (CHCs). A StatCom based on CHCs will be denoted as a H-StatCom.

The H-StatCom topology was chosen for the following reasons:

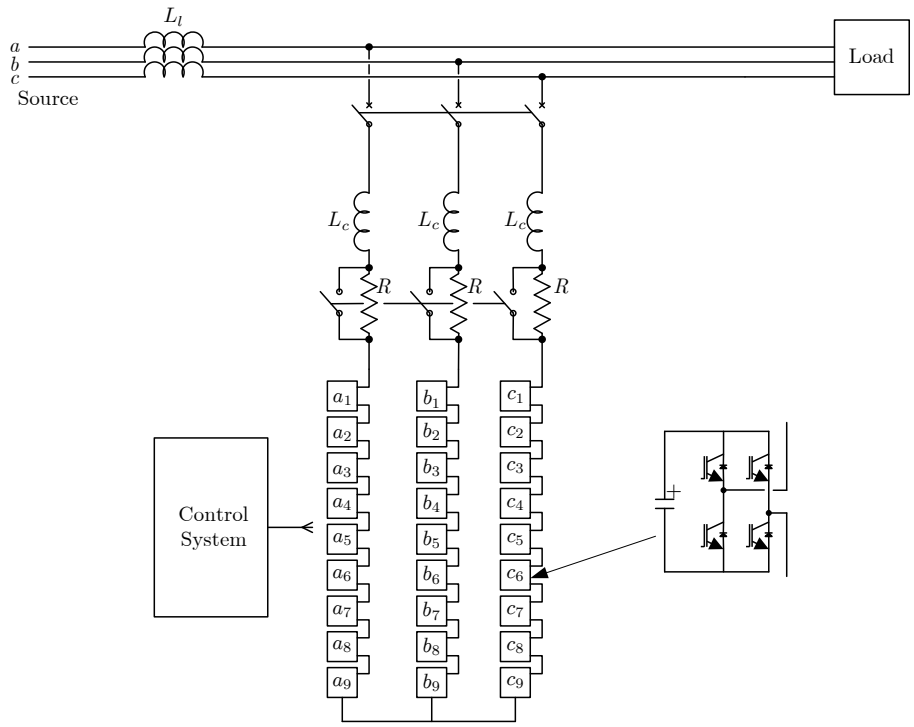

Fig. 1: Conceptual diagram of the structure of the H-StatCom and its connection to the grid.

- The component number for a H-StatCom scales linearly with the number of levels in the converter (other multilevel topologies scale quadratically) [1];
- Voltage balancing can be solved for high level numbers with the H-StatCom [2, 3]. For other multilevel topologies the voltage balancing problems become intractable for high level numbers;
- The H-StatCom is ideally suited to VAR and active filtering applications as it does not have to handle real power. Therefore the complex isolated power supplies required for real power applications are not necessary;
- The H-StatCom is built of identical modules, which means that construction and maintenance of the H-StatCom is simplified. In addition redundancy is easy to build into the unit;
- The high level number possible with the H-StatCom means that direct connection (i.e. no transformer) to distribution level (and above) voltages is feasible. This allows the elimination of the bulky, expensive and lossy transformer;
- The high number of levels available allow more degrees of freedom with respect to harmonic elimination. In addition the filtering required between the H-StatCom and the grid is reduced in size compared to other multilevel topologies;
- As voltage levels increase, more modules of the same voltage and current rating can be stacked, and the MVAR rating of the H-StatCom increases linearly.

The H-StatCom being developed is wye connected to minimise the voltage rating required for the phase legs. It is intended to directly connect the system to an 11kV line-to-line voltage. It is going to use 1.7kV IGBTs as the main power devices. This means that nine series H-bridges per phase leg will be required to give a DC link voltage on each H-bridge of approximately 1.1kV. Fig. 1 shows a conceptual diagram of the overall structure of the H-StatCom, its connection to the grid via inductors and a contactor bypass charging resistor circuit.

The presence of a large number of series connected switches and/or diodes in this topology means that there is a significant cumulative voltage drop across the devices. For example, typical voltage drops across a switched on IGBT of 1.7kV rating is of the order of 2 Volts or more. Since there is the possibility of two switches being on the conduction path this means that there could be a voltage drop of up to

18 volts for the 9 H-bridges. Even if the H-bridges are commanded to output zero voltages the actual voltage at the terminals of each H-bridge will be the voltage drop of one switch and one diode.

The consequences of the above-mentioned voltage drops can have a significant effect on the performance of a H-StatCom, especially if a predictive current control strategy is used. A technique to alleviate this issue is the main focus of this paper.

The Current Control Strategy

The current control strategy used for the University of Newcastle H-StatCom is based on a predictive (or dead beat) current controller [4, 5]. This current control strategy has the advantage of very high bandwidth, simple digital implementation, and only requires the use of instantaneous sampled values. It has been very successfully applied to variable speed drive systems, but its application to H-StatComs is novel. The basic expressions for this control strategy (for the respective dq axes), when applied to the H-StatCom application are:

$$v_{k+1}^{\text{ref}} = \frac{L}{T}(i_{k+1}^{\text{ref}} - \hat{i}_k) + \hat{v}_{k+0.5}^{\text{sys}} \quad (1)$$

$$\hat{i}_k = i_{k-1} + \frac{T}{L}(v_k - v_{k-0.5}^{\text{sys}}) \quad (2)$$

where the "$\hat{}$" symbol denotes an estimated value, and $k \pm 0.5$ denotes in the middle of the next and current control intervals respectively, T is the control period, and L is the connection inductance. The implementation differs from that used in variable speed drives in that it does not use the estimated back-emf, but instead an estimate of the grid voltage in the interval that the control is applied. This estimate is denoted by $\hat{v}_{k+0.5}^{\text{sys}}$, and is the estimated grid system voltage in the middle of the next control interval. This could be estimated using linear interpolation, but a much more accurate technique involves using a digital PLL, which by virtue of its implementation generates a one step ahead estimate. It should be noted that the $v_{k-0.5}^{\text{sys}}$ is an *actual* measurement of the grid voltage in the middle of the control interval where the control calculations are actually occurring.

One issue with the predictive current controller, which is of particular importance in the H-StatCom implementation, is the use of the desired converter output voltage v_k in (2). The implicit assumption is that the desired voltage is actually produced by the converter. As mentioned in the introduction, in the H-StatCom case, the large number of series devices means that the voltage error introduced by device voltage drop can be significant. This results in the actual applied voltage having a significant error with respect to the desired applied voltage, with a consequent error in the predicted current $\hat{i}_k$. This consequently results in an incorrect v_{k+1}^{ref} for the next interval, which in turn is not produced correctly due to the device voltage drops. The applied voltage error results in the desired current i_{k+1}^{ref} not being achieved.

The predictive current controller itself does not have any implicit, or explicit, integrator to eliminate the error introduced by this unknown offset. Even it it did, the offset generated can, in principle, change from control interval to control interval in the multilevel application, making an integrator ineffective.

The Voltage Offset Problem and its Solution

The implemented voltage generation algorithm is really an integrated voltage balancing and PWM algorithm. Therefore in each control interval, based on the direction of the current and the required input charge to each H-bridge capacitor, the algorithm chooses which H-bridges to use to generate the required voltage and even spread the phase leg voltage amongst the H-bridge capacitors. In addition, one of the bridges is PWM'ed to give an even more accurate output voltage. The H-bridges produce two different

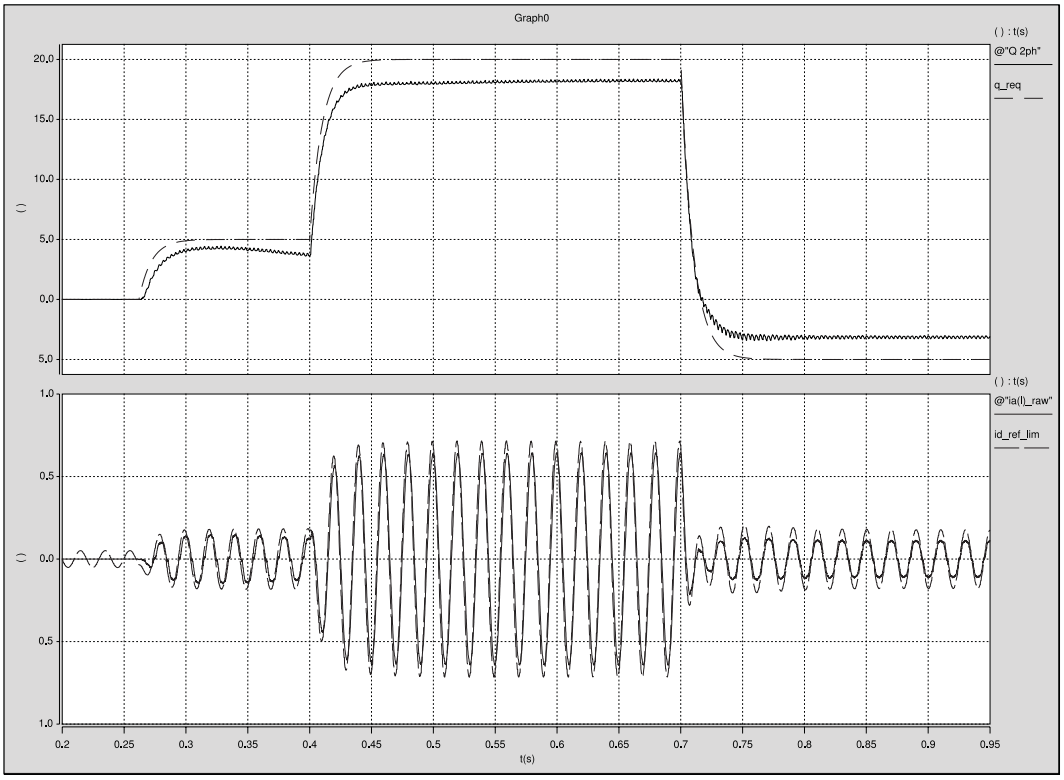

Fig. 2: Simulated of H-StatCom with diode drops in the H-bridges of 0.2 Volts. No voltage compensation.

types of voltage offset – the offset due to the conduction drops when the H-bridge is supposed to be producing zero volts output, and the voltage offset due to the switch drops when the H-bridge is producing a positive or negative voltage. The total phase leg offset is a combination of these two, its specific value related to how many bridges are active and inactive.

Fig. 2 is the result of a simulation of the scaled model H-StatCom briefly described in section . As can be seen from this figure, the offsets generated by the device drops result in a significant relative error in the current, and a consequent error in the the VArs produced (note that there is no feedback on Q in this example). In this particular simulation the voltage drops for the diodes and switches in the circuit are a modest 0.2 Volts.

Remark 1 *It should be noted that the reference current is composed of two components – a real component corresponding to the current that controls the real power flowing to the phase legs, and the other component controls the imaginary power. Feedback control loops on Q and the phae leg voltages (for real power control) will eventually correct the accumulation of errors, but these loops are usually not very fast. Therefore the current error can significantly affect the accuracy of transient current changes. In addition, because the real power component of the current is small, the relative error introduced into this current is large making the real power control less effective.* ■

Remark 2 *The output voltage offset effectively introduces a phase shift in the current relative to the desired current. This occurs when there is a phase shift between the current and voltage (which is* 90° *in the StatCom application) since the offset voltages will be subtractive in one quarter cycle and additive in the other quarter cycle. This phase error affects the real power flow to the StatCom.* ■

Remark 3 *The previous remarks indicate that the accounting for the voltage offsets under zero and non-zero voltage output from the phase legs is essential to have accurate control of the cumulative phase leg voltages.* ■

Voltage offset evaluation

The following offsets types are present in the H-bridge voltages:

- A zero voltage offset when the H-bridge is supposed to be producing zero volts.
- An offset when the bridge is producing an active positive or negative voltage.
- The variable offset due to one of the bridges being PWM'ed with a particular duty cycle.

Remark 4 *It should be noted that the offsets are all dependent on the direction of the current. In the following expressions the current is positive if it flows from the bridge to the grid network (corresponding to a generator power convention).* ■

It can be shown that the total zero offset voltage for the the N bridges in a phase leg is:

$$v_{\text{zoffset}} = N v_{\text{zo}} = N[\underbrace{-(\text{sign}(i)(v_d + v_{\text{on}}) + i(R_d + R_{\text{on}}))}_{v_{zo}}] \tag{3}$$

where i is the current flowing to the phase leg, v_{zo} is a single H-bridge zero volt offset, v_d is the drop across a H-bridge diode, v_{on} is the constant on-state voltage drop of a H-bridge switch, N is the total number of bridges in the phase leg, R_{on} is the on-state resistance of a H-bridge switch, and R_{d} is the resistance of a H-bridge diode in forward conduction.

It follows from (3) that when power flows out of the leg into the load (i.e. is positive) then the zero offset has an opposite direction to that of the total leg voltage. To compensate for the zero offset effect, a higher magnitude total voltage should be produced by the H-bridges in the leg. Similarly, when the power flows into the leg (i.e. is negative) then a smaller magnitude total voltage is required from the leg bridges to compensate for the zero offset effect.

If the H-bridge is intended to produce a non-zero voltage, then the terminal voltage of the H-bridge is:

$$\text{sign}(p)\text{+ve} : v_c^{\text{eff}} = v_c - 2(v_{\text{on}} + \text{sign}(i) i R_{\text{on}}) \tag{4}$$

$$\text{sign}(p)\text{−ve} : v_c^{\text{eff}} = v_c + 2(v_d + \text{sign}(i) i R_{\text{d}}) \tag{5}$$

where v_c denotes the voltage on the individual H-bridge DC link capacitor, p is the power into ($\text{sign}(p)-$ ve) or out of ($\text{sign}(p)+$ ve) the H-bridge, and v_c^{eff} denotes the "effective" DC Link capacitor voltage. In the case of positive power into the phase leg the magnitude of the "effective" capacitor voltage is $v_c - 2(v_{\text{on}} + |i|R_{\text{on}})$ (i.e. less than v_c), and in the case of the negative power $v_c + 2(v_{\text{d}} + |i|R_{\text{d}})$ (i.e. greater than v_c).

To get an insight into the effects of the voltage offsets on the total voltage produced by the phase leg, the following *approximate continuous time model* can be adopted. Assume that all the capacitors in the phase leg are of equal capacitance and are initially charged to $(K_c V_m/N)$, where V_m is the phase voltage amplitude and $K_c > 1$, which means that the total phase leg voltage is greater that the supply (this is a normal condition to allow the current to be controlled). Further assume that the individual capacitor voltages in the phase leg are kept constant and at their initial level by a voltage balancing algorithm. In reality, a small magnitude double frequency oscillation is present on top of the constant capacitor voltage, which can be reduced by using larger capacitance values. Then, given that the control interval is very small (in the extreme case - approaches zero), all the H-bridges in the phase leg will contribute equally to the total phase leg voltage, and the duty cycle of each H-bridge, in average sense over a number of control periods, will closely follow the phase leg voltage:

$$D(t) = v_{\text{leg}}^{\text{ref}}(t)/(N\,v_c(t)) \cong v_{\text{leg}}^{\text{ref}}(t)/(K_c V_m) \tag{6}$$

If the above mentioned offsets in the H-bridge voltages are not compensated for, then the actual phase leg voltage will equal to:

$$v_{\text{leg}}(t) = N\,D(t)\,v_c^{\text{eff}}(t) + N\,(1-|D(t)|)\,v_{\text{zoffset}} \tag{7}$$

where the first term accounts for the capacitor voltages and voltage offsets when the bridges are active and the second term describes the zero offset voltages when the bridges are supposed to produce zero volts. Substituting (3), (4) and (5) into (7) and manipulating, one obtains:

$$\begin{aligned} v_{\text{leg}}(t) =& N\,D(t)\,v_c(t) - N\,\text{sign}(i)(v_{\text{on}}+v_{\text{d}}) - N\,i(t)(R_{\text{on}}+R_{\text{d}}) + \\ & - N\,D(t)(v_{\text{on}}-v_{\text{d}}) - N\,D(t)\text{sign}(i)i(t)(R_{\text{on}}-R_{\text{d}}) \end{aligned} \tag{8}$$

The first term in the above expression, according to (6) yields the reference phase leg voltage. The second term is a constant bias with the sign depending on the sign of the phase current. It averages zero over a period of the generated 50 Hz signal, however, it distorts the voltage waveform. The third term in (8) is in phase with the leg current and thus relates to the active power drawn by the StatCom even in the case of a purely reactive load. The fourth term is in phase with the reference voltage and affects the generated voltage magnitude. The fifth non-linear term also affects the voltage magnitude as well as contributes a double frequency oscillation component to the generated waveform.

From all the above it follows that the non-compensated H-bridge offsets:

1. Change the phase voltage magnitude and shift its phase.
2. Create an active power component in the StatCom related to the resistance losses.
3. Distort the voltage waveform.

With a large number of H-bridges in one leg, these effects can be significant, as shown by the simulation and experimental results included in this paper. Therefore, for accurate and non-distorted StatCom operation the voltage offsets of all types need to be compensated for.

Voltage offset compensation

The compensated voltage balancing/PWM algorithm is sequenced as follows[1]:

1. Calculate the v_c^{eff} using (4) or (5).
2. Order the v_c^{eff} in order from the lowest voltage to the highest voltage.
3. If $p > 0$ then reverse the order of the v_c^{eff} array.
4. Starting with the first H-bridge in the array, calculate the duty cycle for the bridge (using the expression below). Continue this in a loop through the array whilst the duty cycle for the nth bridge is $|D_n| > 1$ and $\Sigma_{i=0}^{n-1} D_{i-1}(v_{c_i}^{\text{eff}}) < v_{k+1}^{\text{ref}}$, where the first H-bridge has an index of zero. If $n = N-1$ then all bridges are required and none are PWM'ed.
5. If $|D_n| > 1$ then limit as $D_n = \max(-1, \min(1, D_n))$.
6. The duty cycle is then using used to fire the respective H-bridges in the phase leg, and the the H-bridge with $|D_n| < 1$ generates a symmetrical PWM output.

[1] Note that this sequence is repeated at the control rate, which is every 400μsecs in the prototype system.

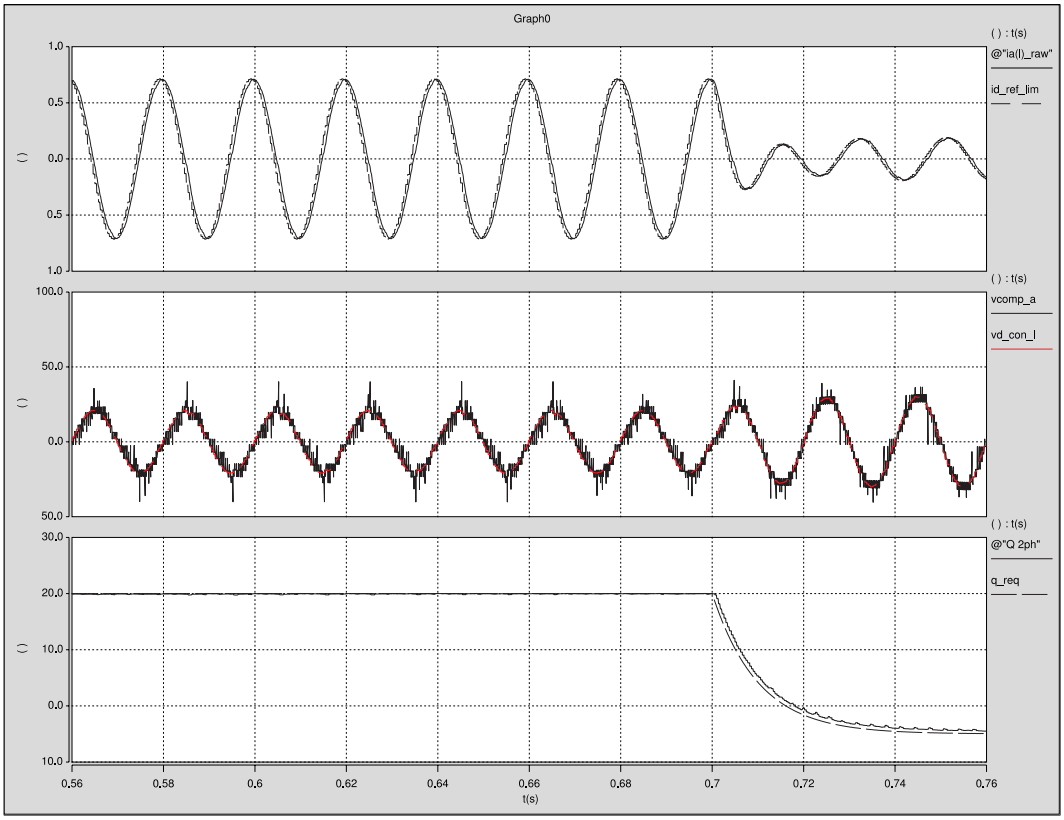

Fig. 3: Simulation under equivalent conditions shown in Fig. 2 but with offset compensated algorithm.

The duty cycle D_n is developed from the basic expression:

$$v_{k+1}^{\text{ref}} = \Sigma_{i=0}^{n-1} D_{i-1} v_{ci}^{\text{eff}} + D_n v_{cn}^{\text{eff}} - v_{\text{zoffset}}^{\text{eff}} \tag{9}$$

where $v_{\text{zoffset}}^{\text{eff}} = (N-n-|D_n|)v_{\text{zo}}$. The full derivation, which is relatively straight forward manipulations, will be stated without proof due to paper length limitations :

$$D_n = \frac{v^* - \Sigma_{i=0}^{n-1} D_{i-1} v_{ci}^{\text{eff}}\big|_{n>0} - (N-n)v_{\text{zo}}}{v_{cn}^{\text{eff}} - \text{sign}(v^* - \Sigma_{i=0}^{n-1} D_{i-1} v_{ci}^{\text{eff}}\big|_{n>0} - (N-n)v_{\text{zo}})v_{\text{zo}}} \tag{10}$$

where D_n is a signed duty cycle indicating the polarity of the bridge.

Fig. 3 shows the results of a Saber simulation with the compensated voltage balance/PWM algorithm. The conditions for this simulation were exactly the same as that for Fig. 2. As can be seen the current waveform no longer has the offset error. Closer inspection of these waveforms reveals that the current is almost exactly following the reference. The spikes on the voltage waveform are due to the dead-time in the inverter, and manifest themselves because of the voltage balancing algorithm. A technique to eliminate these spikes is the subject of a companion paper at this conference.

Experimental Results

In order to validate the simulation studies, the ‘C’ code dll used in the Saber simulation was converted for operation in the real-time control environment for a low voltage (415VAC) 19 level H-bridge StatCom.

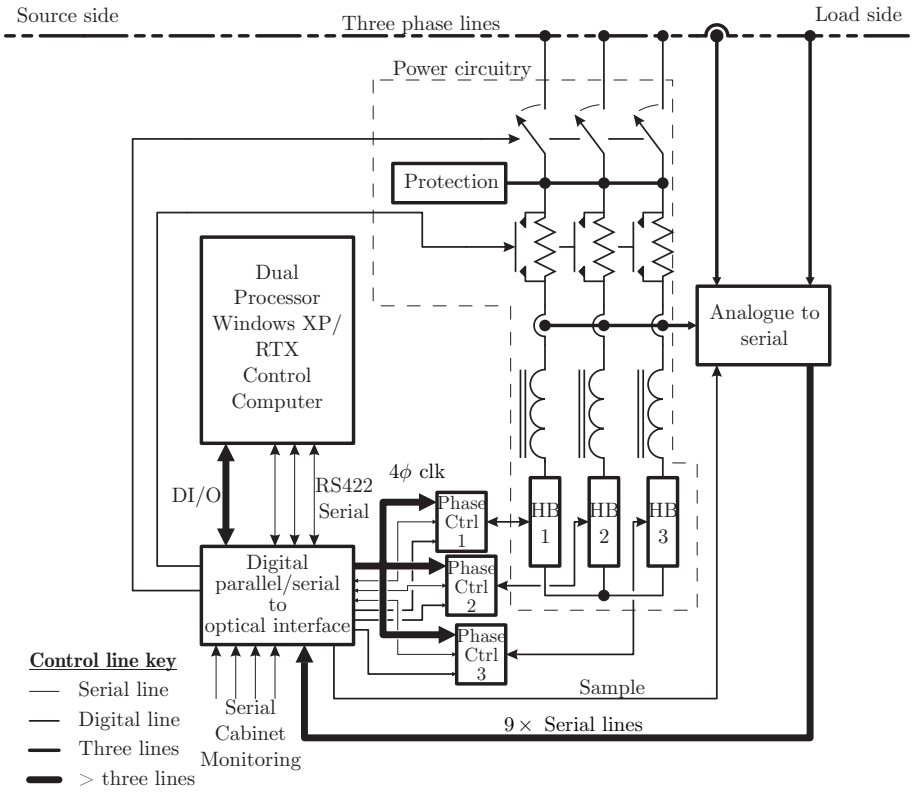

Fig. 4: Block diagram of the experimental system.

The StatCom used for the experimental results is a scaled model of an 11kV StatCom. It has 9 H-bridges per phase, with each H-bridge designed with MOSFET power devices. The phase legs are wye connected. A block diagram of the experimental system appears in Fig. 4. One can see that it is implemented as a multi-processor system, with individual processors implementing the control of each of the phase legs. These phase leg processors receive the desired output voltage from the current control algorithm, which is implemented in a central Windows XP system. It is the individual phase leg processors where the converter drop compensation and PWM algorithm have been implemented. Fig. 5 is photograph of the laboratory set-up showing the individual pieces of equipment.

The parameters for the StatCom legs used for the experiments were: the on-state and diode drops $= 0.2$V; and the on-state resistance of the MOSFETs was 0.028Ω. An experiment was run to produce 20Vars[2], and the plots of the reference and actual currents for phase 'a' appear in Figs. 6 and 7 respectively. Fig. 6 is for the case where the inverter leg voltage drops are not modelled. As can be seen there is a considerable error between the reference and the actual current being produced. One can also see the phase shift mentioned previously between the reference waveform and the actual current waveform. This corresponds well with the simulation result shown in Fig.2, where one can see that there is a similar relative error. The experiment was repeated with the compensated PWM algorithm and the plots of Fig. 7 resulted. Compared to Fig. 6 the reference current is being tracked much more accurately, with only a sample delay between the reference and the output current. Again there is excellent correspondence between this experiment and the simulated output shown in Fig. 3.

Conclusions

This paper has developed a combined capacitor voltage balancing and converter voltage drop compensation algorithm for use in cascaded H-bridge multilevel StatComs. The algorithm is suitable for use with predictive current control of a H-StatCom. The effects of converter voltage drops on the accuracy

[2]The power level is very low as this unit is still in the initial commissioning phase.

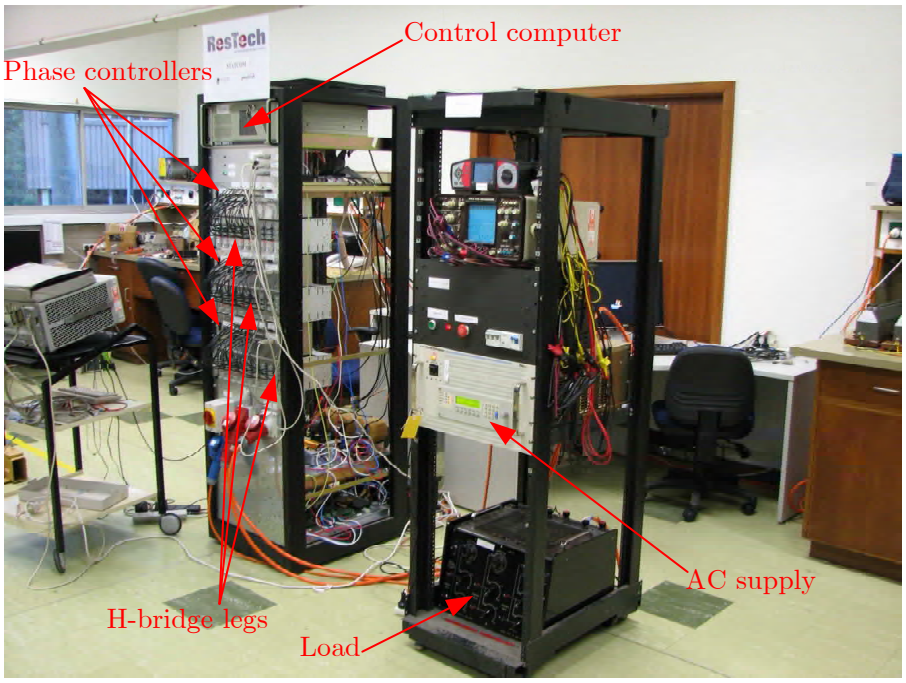

Fig. 5: Photograph of the 19 level experimental StatCom.

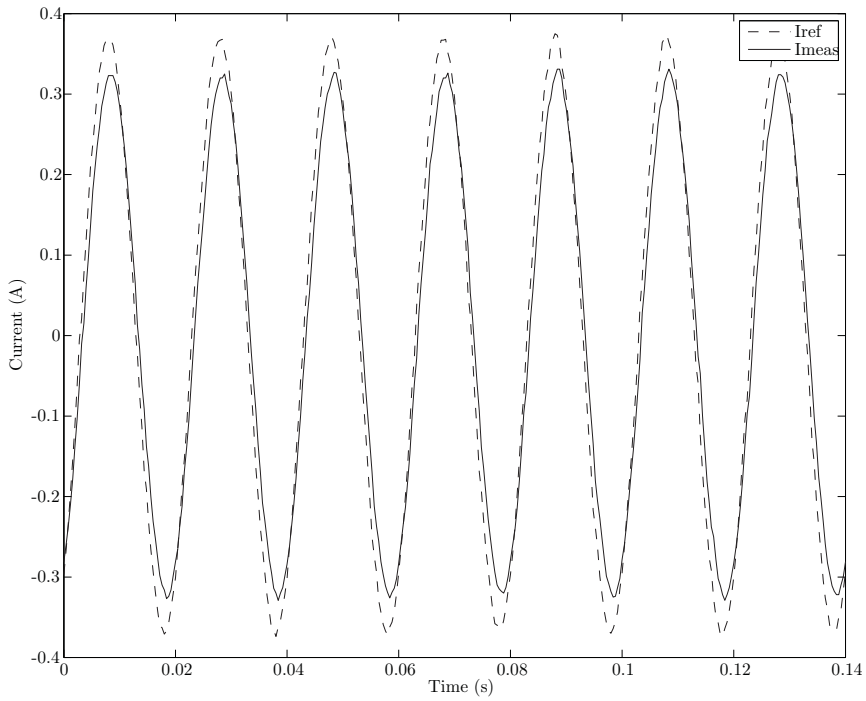

Fig. 6: Experimental results from the 19 level StatCom *without* modelling of the converter losses.

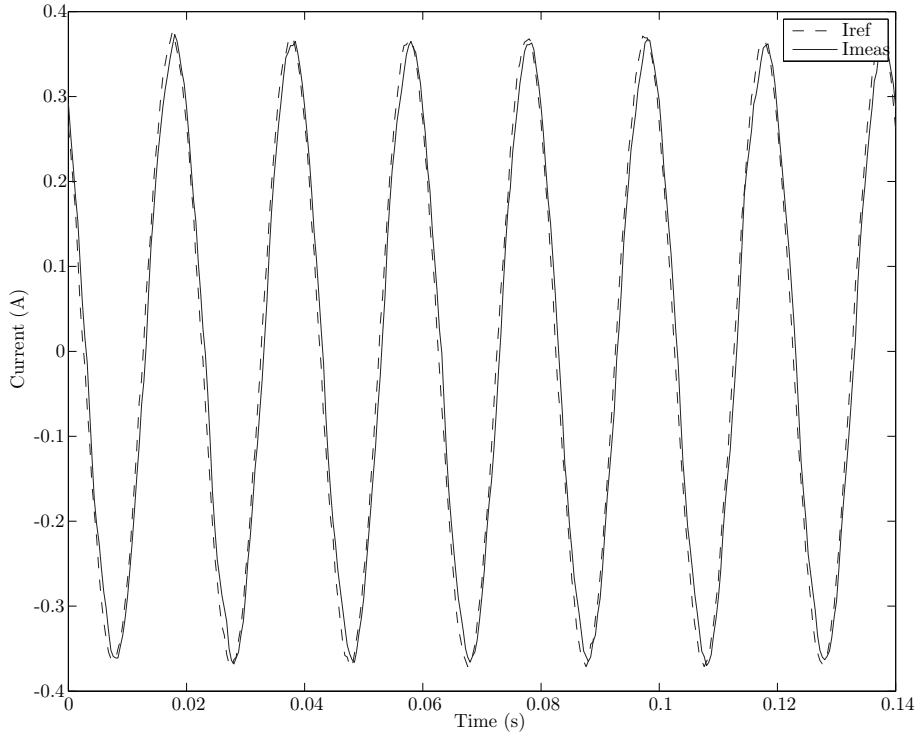

Fig. 7: Experimental results from the 19 level StatCom *with* modelling of the converter losses.

of the current produced with predictive current control were investigated. It was shown that substantial magnitude and phase errors result between the reference current and the actual current.

The new combined voltage balance and PWM algorithm that models the converter drops during each control interval was developed. It generates a compensated PWM duty cycle that accounts for these drops so that the desired output voltage (and therefore output current) is achieved. The excellent performance of this algorithm was verified by simulation and experiments on a 19 level H-bridge StatCom.

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